Abstract of the Disclosure

A semiconductor memory device is capable of enhancing a sensing speed at a central region of a bit-line sense amplifier array by multiplying output lines of a sense amplifier driver. For the purpose, the semiconductor memory device includes a sense amplifier array unit including a plurality of bit-line sense amplifiers arrayed to each other, a first driver, located at one side of the sense amplifier array unit, for generating a driving voltage of the plurality of bit-line sense amplifiers, a second driver, located at the other side of the sense amplifier array unit, for producing the driving voltage of the plurality of bit-line sense amplifiers, a first power line, which is connected between an output node of the first driver and that of the second driver, and to which a driving voltage input node of each of the plurality of bit-line sense amplifiers is attached in parallel, and a second power line, connected to the first power line in parallel between the output node of the first driver and that of the second driver, and strapped with the first power line at least one point.